In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A processing device comprising:

a processing module capable of multitasking multiple tasks;

one or more associated circuits, which may be selectively configured responsive to control signal, coupled to said processing module, said one or more associated circuits includes a cache configuration circuitry for configuration of a cache; and

a memory storing ~~a control word~~ task attribute bits for configuring the ~~associated circuits~~ cache via the cache configuration circuitry, wherein each task has an associated ~~control word~~ task attribute bit which is stored in the memory while the task is being executed by the processing module.

2. (Currently Amended) The processing device of claim 1 wherein said ~~control word~~ task attribute bits comprises a plurality of fields.

3. (Original) The processing device of claim 2 wherein each of said associated circuits has an associated field.

4. (Original) The processing device of claim 3 wherein each of said associated circuits has configuration circuitry for configuring the associated circuit responsive to a value stored in said associated field.

Claims 5 to 13. (Canceled)

14. (Original) The processing device of claim 1 wherein said processing module comprises a first processing module, and further comprising one or more additional processing modules.

15. (Currently Amended) A method of operating a processing device including a processing module capable of multitasking multiple tasks coupled to one or more associated circuits, said one or more associated circuits includes a cache configuration circuitry for configuration of a cache, comprising the steps of:

identifying a current task; and

storing ~~a control word~~ task attribute bits associated with said current task in a memory; and

configuring the ~~associated circuits~~ cache circuitry via the cache configuration circuitry to a state responsive to the ~~control word~~ task attribute bits during execution of said current task.

16. (Currently Amended) The method of claim 15 wherein said storing step comprises the step of storing ~~a control word~~ task attribute bits having a plurality of predefined fields.

17. (Currently Amended) The method of claim 16 wherein each of said associated circuits has an associated field in said ~~control word~~ task attribute bits.

18. (Original) The method of claim 17 wherein said enabling or disabling step comprises the step of configuring each of the associated circuits responsive to a value stored in said associated field.

Claims 20 to 23. (Canceled)

24. (Currently Amended) The method of claim 15 wherein said processing module includes a plurality of processing subsystems and further comprising the step of configuring said processing subsystems responsive to said ~~control word~~ task attribute bits.

Claims 25 and 26. (Canceled)

27. (New) The processing device of claim 1, wherein:

said cache includes a plurality of selectively configurable cache ways; and

said cache configuration circuitry configures said cache ways according to said task attribute bits.

28. (New) The processing device of claim 1, wherein:

said cache includes a plurality of selectively configurable data paths; and

said configuration circuitry configures said cache data paths according to said task attribute bits.

29. (New) The method of claim 15, wherein:

said step of configuring the cache circuitry via the cache configuration circuitry configures cache ways according to the task attribute bits.

30. (New) The method of claim 15, wherein:

said step of configuring the cache circuitry via the cache configuration circuitry configures cache data paths according to said task attribute bits.